charges is q, a dielectric constant of the vacuum is ε, a relative dielectric constant of silicon is ε', and impurity concentration N_D of P-type diffusion region 7 is sufficiently larger than impurity concentration N_A of N^--type epitaxial layer 2, and is substantially infinite, the following formulas must be satisfied.

$$V > qN_DW^2/(8\varepsilon\varepsilon')$$

$$W < 2(2V\varepsilon\varepsilon'/(qN_D))^{(1/2)}$$

As shown in Fig. 3, the distance W between neighboring P-type diffusion regions 7 satisfies the foregoing relationships, whereby rising of the on resistance in the on state can be suppressed while keeping the effect of reducing the electric field.

Please replace the paragraph beginning at page 16, line 28, with the following rewritten paragraph:

In this semiconductor device, each P-type diffusion region 7 is fixed to the source potential. In particular, as shown in Fig. 23, each P-type diffusion region 7 is electrically connected to source electrode 9 via a contact hole 15, which is formed in silicon oxide film 20 and exposes the surface of corresponding P-type diffusion region 7. In alternative embodiments, each P-type diffusion region 7 is electrically connected to gate electrode 8a. Structures other than the above are substantially the same as those of the semiconductor device shown in Fig. 1. The same parts and portions bear the same reference numbers, and description thereof is not repeated.

IN THE CLAIMS:

Please amend claim 1 as follows:

1. (Amended) A semiconductor device comprising: